Trigger Electronics Upgrade of PHENIX Muon Tracker

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Abstract

The Relativistic Heavy Ion Collider (RHIC) at Brookhaven National Laboratory (BNL) provides a unique opportunity to collide polarized protons at high energies. One of the highlights of the polarized proton program at $\sqrt{s} = 500$ GeV is the direct measurement of sea quark contribution to the proton spin via $W$-boson production by measuring parity violating single spin asymmetry. A new trigger electronics on forward muons which specializes in $W$-boson detection was developed for the PHENIX experiment. The trigger was installed as an additional electronic circuit which is connected in parallel to existinig cathode readout electronics of the muon tracking chamber.

Keywords: $W$-production with minimal theoretical uncertainties. Sub-leading twist and higher-order terms in the perturbative QCD expansion are strongly suppressed, and a direct extraction without additional assumptions becomes possible [1]. This program thus will break new ground in our detailed understanding of the proton’s structure. Especially, our present knowledge for the anti-quark contribution to the proton spin is limited with larger uncertainties to measurements by semi-inclusive deep-inelastic scattering (SIDIS). In addition to aforementioned naturally set high energy scale, the sea quark measurement via $W$ has certain advantages compared to SIDIS in following sense: 1) The $W$ boson couples with the quark flavor selectively, and quarks (anti-quarks) with negative (positive) helicity can participate in the reaction due to the $V-A$ structure of the weak interaction, 2) free from fragmentation function which is the unavoidable dominant source of model uncertainties for SIDIS on their way to extract the sea quark polarization from observed asymmetries. Because the measurement of $W$ asymmetry in forward/backward angle give large probability of kinematics of unbalanced Bjorken $x$’s from two colliding protons, the measurement of $W$ asymmetry in forward/backward angle further enhances the sensitivity to the sea-quark polarization.

The $W$ program was initiated by the first operation of RHIC polarized proton beams at its highest operational energy $\sqrt{s} = 500$ GeV in 2009. This $W$ program is the highlight of RHIC spin project for the next five years and thus following upgrade

1. Introduction

A new trigger on forward high-momentum muons for the PHENIX experiment was developed for the purpose of measuring longitudinal spin asymmetry in $W$ boson production at polarized proton-proton collisions with $\sqrt{s} = 500$ GeV at RHIC. The measurement provides a direct probe to the individual polarized parton distribution function (PDF) of the quarks and anti-quarks in the proton. Since the muon trigger before the upgrade fired on any muons above 2 GeV/c, it was inefficient to trigger high-momentum muons from $W$ decays and did not provide the required trigger rejection factor for 500 GeV running. The new system performs coarse online tracking and triggers events with high-momentum particles by selecting straight tracks in a magnetic field. It suppresses a large number of background events of low momentum muons coming from hadronic decays. Three major upgrade projects are parts of the new trigger; (1) Resistive plate chambers (RPC1 and RPC3) [2], (2) Upgrade of muon trigger front-end electronics (muon trigger front-end electronics, MuTRG-FEE) [3], (3) Additional hadron absorber. We discuss (2) in this article.

1.1. Physics motivation

Parity-violating production of the $W$ boson with longitudinally-polarized proton-proton collisions at RHIC provides a direct measure of the individual polarizations of the quarks and anti-quarks in the colliding protons. The high energy scale set by the $W$-mass makes it possible to extract quark and anti-quark polarizations from inclusive lepton spin asymmetries in $W$-production with minimal theoretical uncertainties. Sub-leading twist and higher-order terms in the perturbative QCD expansion are strongly suppressed, and a direct extraction without additional assumptions becomes possible [1].
projects to PHENIX muon arms have been pursued to prepare for the rare probe measurement under high-background rate circumstances.

1.2. RHIC polarized proton beam

RHIC [4] consists of two counter rotating accelerator/storage rings with six beam crossings points labeled as 2,4,6,8,10, and 12 o’clock where collisions may take place. Each rings are built on a common horizontal plane, one (“Blue Ring”) for clockwise and the other (“Yellow Ring”) for counter-clockwise beams. Each RHIC ring is capable of being loaded with 120 bunches (9.4 MHz) apart. This timing pulse is called the RHIC beam clock and distributed to experiments in order to let readout system of detectors to be synchronized with the collision timing.

1.3. PHENIX and preexisting muon arm detector

The PHENIX detector [5] is a large multipurpose set of detectors optimized for measuring rare electromagnetic probes (photons, muons, and electrons) of the spin structure of the proton and of the hot dense matter created in ultra-relativistic heavy ion collisions. The data acquisition system and multi-level triggers are designed to handle the largely different challenges presented by $p + p$ collisions (relatively small data size per event at very high rates) and Au+Au collisions (very large data size per event at relatively low rates) with little or no dead time [7, 8]. Event characterization devices, such as the Beam-Beam Counters [9], provide information on the vertex position, start time, and centrality of the collision. The two muon arms, shown in Fig. 1, which specialize in muon detection cover 1.2 < $|\eta|$ < 2.4 in pseudorapidity and $\Delta \phi = 2\pi$ in azimuth which results in acceptance of almost 1 sr.

![Figure 1: The PHENIX muon arm detection system and new devices to upgrade the trigger performance of the muon arms. New devices are given their names and year of the installation.](image)

Each MuTr arm consists of three stations (named Station-1, Station-2, and Station-3 proceeding downstream from the collision vertex) of cathode-readout strip chambers. They are installed in an eight-sided conical magnet [10] which provides the radial magnetic field ($\int B \cdot dl = 0.72$ T-m at 15 degrees, $B(\theta) \approx B(15^\circ) \tan(\theta/\tan(15^\circ))$) and bends particles in the azimuthal direction. Each MuTr station occupies a plane perpendicular to the beam axis and also partitioned into identical eight segments called “octant”. The octant consists of multiple ionization gaps of an anode plane sandwiched by two cathode planes; three gaps for the two stations closest to the collision vertex and two gaps for the last station. The anode planes are alternating structures of 20 µm-diameter gold-plated tungsten sense wires and 75 µm-diameter gold-plated copper-beryllium field wires. Each wire is running along the azimuthal direction with a sense wire spacing of 10 mm. Cathode planes are segmented into strips of 5 mm pitch with readout alternately. Half of the cathode planes have strips oriented perpendicular to the anode wires (non-stereo planes) and the other half have strips with a small stereo angle of 11.25 degree or less (stereo planes) to provide two-dimensional information. The chamber gas mixture is 50 % Ar + 30 % CO₂ + 20 % CF₄. Typical operating high voltage is 1900 V with a gain of approximately $2 \times 10^7$. An ionizing particle typically fires three adjacent strips in each orientation to form “cluster”. A fit to the charge profile on the cluster provides a position measurement with a designed resolution of about 100 µm in the bend direction.

Each MuID arm consists of five steel absorber plates interleaved with Iarocci tubes[14] operated in proportional mode and specialized shielding to reduce backgrounds not originating from the collision vertex. The first MuID absorber plate (thickness = 20 cm - South; 30 cm - North) also serves as the return yoke of the MuTr magnet. Successive plates (identical for the two arms) are 10, 10, 20 and 20 cm thick, thus totaling $4.8 \lambda/I / \cos \theta (5.4 \lambda/I / \cos \theta)$ for the South (North) arm, where $\lambda/I$ indicates the nuclear interaction length and $\theta$ is the polar angle of a particle’s trajectory. Gaps are labeled 0 to 4 proceeding downstream from the collision point. Each gap consists of horizontal and vertical Iarocci tubes with ~8 cm width and 2.5 –
5 m length to provide coarse two-dimensional position. Tracks which penetrate all MuID steel plates and point to the collision vertex are identified online and triggered as conventional PHENIX muon arm trigger.

1.4. Trigger upgrade
1.4.1. Overview

The trigger for the muon arms before the upgrade was generated by MuID. It provides the rejection power of ~200 compared with the PHENIX minimum-bias trigger by BBC at \( \sqrt{s} = 200 \) GeV.\(^1\) The RHIC design goal of the luminosity is \( 2.0 \times 10^{32} \text{cm}^{-2}\text{s}^{-1} \), which results in about 6 MHz of BBC trigger. In order to meet the typical DAQ bandwidth of 2 kHz allocated for the PHENIX muon arm, the rejection power of 3000 is required. Based on a prediction that the rejection power by MuID will not be so much different between 200 GeV and 500 GeV, the MuID trigger wouldn’t be sufficient to trigger \( W \) without pre-scaling.

The momentum threshold of the MuID trigger is \( p_T \sim 1.5 \text{ GeV/c} \) (~2.8 GeV/c in momentum), while the typical muons decay from \( W \) boson dominates the single muon yields at high transverse momentum region \( p_T \gtrsim 15 \text{ GeV/c} \) with respect to background muon sources as shown in Fig. 2. Based on this fact, raising the threshold even higher leads to the efficient trigger of the signal with sufficient rejection power. Here we introduced a new momentum-sensitive trigger by adding new fast readout electronics (muon trigger front-end electronics, MuTRG-FEE) to existing MuTr front-end electronics. MuTRG-FEE digitize the signal immediately and therefore deal with only hit information providing fast and coarse online tracking information of the traversing particle in MuTr to back-end trigger logic circuit. Events with high-momentum charged particles are triggered based on the online tracking results.

However, due to the limited intrinsic timing resolution of MuTr (approximately 2 – 3 beam clocks), the other timing detector with sufficient timing resolution is needed to identify the beam clock which collision bunch an observed hit comes from. BBC can be such a timing detector and we evaluated MuTRG-FEE performance in collaboration with BBC for this article. However, the situation will be more serious at high collision rate where BBC will start triggering every events and will not determine collision timing. Another new upgrade detector, resistive plate chambers (RPC), will resolve the difficulty taking advantage of its sufficient intrinsic timing resolution of a few ns and low occupancy owing to its small segmentation. If one finds corresponding hit in the RPC at the expected location from the extrapolation of the track observed by MuTRG-FEE, the timing observed by RPC is allocated to the track.

1.4.2. MuTRG-FEE

MuTRG-FEE system utilizes about 5% of signal charge from non-stereo cathode planes of MuTr and extract hit information of the strips. Fig. 3 displays the principle of selecting high-momentum particles using the obtained hit pattern. \( \Delta \text{strip} \) is introduced to be an important parameter to identify high-momentum tracks and is defined as a deviation of hit at Station-1, the new electronics provides the trigger of only high-momentum track.

A block diagram of the new muon trigger system is shown in Fig. 4. A new amplifier and discriminator board (MuTRG-ADTX) are attached to MuTr front-end electronics (MuTr-FEE) and divides the signal into two paths; analog readout path for existing MuTr-FEE and the digitization path for the fast trigger. The digitized signals are sent to new data merger boards (MuTRG-MRG), which are located in the PHENIX rack room and about 70 m far from the collision region. The MuTRG-MRG board collects hit signals from multiple MuTRG-ADTXs and formats the data to meet the input format of the downstream Local Level-1 (LL1) trigger module. To identify tracks which fire the trigger in the offline analysis, the copy of hit patterns transmitted to LL1 from MuTRG-MRG is sent to data collection modules (DCM) via other interface boards (MuTRG-DCMIF). The data are then recorded into PHENIX main data stream. We name MuTRG-FEE as a system which consists of MuTRG-ADTX, MRG and DCMIF. The LL1 module makes trigger decision by comparing hit patterns from MuTRG-MRG and pre-defined look-up table which contains hit combination of high-momentum tracks. The signals from other upgrade detectors, RPCs, can also be merged in the LL1 module. The local trigger decision by LL1 module is finally transmitted to the Global Level-1 (GL1) trigger module, where the PHENIX global trigger is generated in combination with LL1 triggers from other detector systems like MuID and BBC.

\(^1\) We define the trigger rejection power as the number compared to the PHENIX minimum-bias trigger rate by BBC in this article. The cross section observed by BBC is about 30 mb at \( \sqrt{s} = 500 \) GeV, which is about half of the proton-proton total cross section.
Figure 3: The concept of momentum-sensitive trigger using muon tracker cathode strip readouts. A coarse momentum measurement is carried out online by calculating $\Delta$strip, a deviation of hit at Station-2 from the linear interpolation between Station-1 and Station-3 hits. Tracks with small $\Delta$strip are triggered.

Figure 4: The block diagram of the new muon trigger system.

The R&D of these new boards were completed by the end of 2008. The production and installation to North muon arm was completed in 2008 and they were commissioned in the 2009 RHIC Run, whereas South muon arm was completed in 2009 and were commissioned in the 2010 RHIC Run Au-Au collision data as well.

1.4.3. Resistive plate chambers

The PHENIX resistive plate chamber (RPC) has a standard double gap structure and is based on the RPC’s built for the Compact Muon Solenoid (CMS) experiment at CERN. The gas chamber is constructed with two 2 mm bakelite plates ($\sim 10^{10}$ $\Omega$ cm), as resistive plates, with 2 mm gap. The outside surface of the RPC is coated with graphite, which are used as electrodes. A high voltage of $-9.5$ kV is applied to one side of the graphite and the other side is grounded. Readout planes are made from copper strips running along the azimuthal direction to measure an azimuthal position which is sensitive to the track momentum. Gas is 95% C$_2$H$_2$F$_4$ + 4.5% i-C$_4$H$_{10}$ + 0.5% SF$_6$. One of the attractive features of the RPC detector is that the readout plane is completely isolated from the gap chamber. Charge is induced on the readout strip by an avalanche in the gas gap and processed by the readout electronics. Some features of the PHENIX RPC as the new $W$ trigger are listed on Table 1.

Table 1: Characteristics of the PHENIX RPC with $-9.5$ kV supplied.

<table>
<thead>
<tr>
<th>PHENIX RPC characteristics</th>
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<tbody>
<tr>
<td>Cluster size</td>
</tr>
<tr>
<td>Efficiency</td>
</tr>
<tr>
<td>Time resolution</td>
</tr>
<tr>
<td>Rate capability</td>
</tr>
<tr>
<td>Segmentation</td>
</tr>
</tbody>
</table>

Owing to the good timing resolution, RPC plays an important role as a timing device under the high luminosity circumstances substituting for BBC, as well as it provides a strong suppression against cosmic-ray background. RPC prototype was partially installed during RHIC shutdown period in 2008 and commissioned in the 2009 RHIC run with beam collisions. RPC installation behind MuID (RPC3) for both muon arms were completed in the RHIC shutdown period of 2009 and 2010. Additional RPC installation in front of MuTr (RPC1) is being carried out in the 2011 RHIC shutdown period.

1.4.4. Additional hadron absorber

Another piece of the upgrade is a new hadron absorber which is mounted downstream of the MuTr magnet. The 35 cm-thick SS310 absorber plates with 24 tons were manufactured at ATLAS Tool&Die Works, Lyons, IL, USA on contract from the University of Illinois at Urbana-Champaign, USA. SS310 is Cr (24 – 26%) and Ni (19 – 22%) enriched austenite phase stainless steel. It has characteristic of small magnetic permeability of $\sim 10^{-3}$ and thus makes minimum impact to well measured existing magnetic field. By installing the new absorber, the pre-MuTr absorber presents a total thickness of 7.1A/ $\cos \theta$ (was 4.9 before), where $\theta$ is the polar angle of a particle’s trajectory. This absorber reduces the MuTr occupancy and provides the first level of hadron rejection of a factor of about three orders of magnitude. Due to ionization energy loss, a particle must have a momentum at the vertex which exceeds $2.71/ \cos \theta$ GeV/c ($2.85/ \cos \theta$ GeV/c) to penetrate to the most downstream MuID gap of the South (North) arm after new absorbers are installed.

2. MuTRG-ADTX board

MuTRG-ADTX boards are located just next to MuTr and attached to existing MuTr-FEE to deal with raw signal from
The signals are digitized in this board to generate fast
signal for the Level-1 trigger. Main functions of MuTRG-
ADTX are followings.

- Splitting charge from MuTr to two paths, MuTr-FEE and
  MuTRG-ADTX.
- Amplifying and discriminating raw signals.
- Formatting digitized signals to transmit them to the down-
  stream MuTRG-MRG board via an optical cable.

MuTRG-ADTX was developed based on two important guide-
line. One is to minimize impact on performance, position res-
olution and detection effi

ciency, of existing MuTr-FEE. Since
the momentum resolution of a detector like MuTr is increas-
ing quadratically as the momentum of the particle becomes higher,
it is important to keep the MuTr resolution as better as possible
for W-boson detection. The other guideline is to process MuTr
signal fast enough to be in time for the trigger decision with
high efficiency and good timing resolution. A restriction in the
development is that any components affected by magnetic field
are unavailable because MuTRG-ADTX is installed inside or
attached to the muon arm filled with magnetic field. The spec-
ification of MuTRG-ADTX and its chassis are summarized in
Table 2.

2.1. Analog part

MuTRG-ADTX is designed to consume minimal portion of
the signal charge from MuTr to form the trigger primitives,
leaving a large fraction of the charge for the MuTr-FEE to save
the gain as much as possible. A small capacitor of 56 pF (C_split)
is implemented to divide the charge at the input of MuTRG-
ADTX as shown in Fig. 5. Because effective capacitance of the
existing MuTr-FEE is about 900 pF, about 5 % of the charge
from MuTr is transmitted to MuTRG-ADTX and the remaining
95 % of the charge is used by existing MuTr-FEE to provide
precise position information. On the other hand, the additional
capacitance could behave as the new noise source on MuTr-
FEE. The small capacitance for the C_split is preferable in this
sense. Cables connect between MuTRG-ADTX and MuTr-FEE
were employed as short as 30 cm for the most of part from the
same reason above. Another impact of C_split on MuTr-FEE is
delay of signal timing. These impact on MuTr-FEE is evaluate
d in Section 3.1.

The raw signals are amplified and discriminated there and
sent to the digital part of MuTRG-ADTX as the second stage.
Fig. 6 shows the circuit diagram of the MuTRG-ADTX ana-
log part. Since a typical charge deposit on MuTr by a single
charged particle is 100 fC and only about 5 fC can be available
in MuTRG-ADTX, low noise and high gain are preferable. On
the amplifier part, we selected AD8038 and AD8065 op-amp of
Analog Devices which feature high speed and low noise. Pulse
height and peak time after the amplifier is about 300 mV and
200 nsec with 100 fC charge deposit in MuTr. Noise after the
amplifier is about 5 mV in root-mean-square (RMS).

For the discriminator part, we implemented cable-less con-
tant fraction discriminator (CFD) to eliminate time walk ef-
fect as well as nominal leading edge discriminator (LED). CFD
is realized by producing high-pass and low-pass signal from
the original signal and transmitting them to comparator (See
also Fig. 7). The output signal timing of the comparator is de-
termined by the intersection of high-pass and low-pass signal,
which is independent of the pulse height. LED is also gener-
ated by another comparator with the original signal and thresh-
old voltage as inputs. The threshold voltage are provided by
8 bit DAC (Digital-to-Analog Converter) with a range of 0 to
125 mV. Because the timing of the CFD output always delays
by about 250 nsec than the LED output, the timing of the AND
signal of the CFD and LED signal is determined by that of the
CFD signal, as well as its threshold is equivalent to that applied
to the LED signal. In the following text, We describe CFD as
the signal after taking AND of LED and CFD for convenience.

Figure 5: Schematic diagram of the charge split between MuTr-FEE and
MuTRG-ADTX.

Figure 7: Signal shape used for CFD. Measured at test bench.

MuTRG-ADTX board consists of 8-layer substrate and use
of each layer is summarized in Table 3. Although the ground
of analog sector (AGND) and that of digital sector (DGND) have
electrical conduction via ground of voltage regulators, they are
well separated to prevent the noise generated in the digital sec-
tor picked up in the analog sector. The first and the last layer is
Table 2: Specification of ADTX and chassis of ADTX.

<table>
<thead>
<tr>
<th>ADTX</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Board Size</td>
<td>6 U</td>
</tr>
<tr>
<td>Number of channels</td>
<td>64 at maximum</td>
</tr>
<tr>
<td>Supplied Low Voltage</td>
<td>6.2 V (5.7 V at minimum)</td>
</tr>
<tr>
<td>Used Voltage</td>
<td>5.25, 3.3, 2.5, 1.25 V (modulated by regulators)</td>
</tr>
<tr>
<td>Consumption Current</td>
<td>~2.0 A</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>~12.4 W</td>
</tr>
<tr>
<td>Signal Process Time</td>
<td>2.5 – 3.5 beam clocks with LED</td>
</tr>
<tr>
<td></td>
<td>5.2 – 6.2 beam clocks with CFD</td>
</tr>
</tbody>
</table>

Chassis of ADTX

| Size                  | 189 × 267 × 36 mm³ |
| Capacity              | 2 boards           |
| other features        | Water cooling and dry air supply system are equipped. |

Figure 6: The circuit diagram of MuTRG-ADTX analog part. AGND and DGND represents analog and digital ground, respectively. AVCC, DVCC and VREF are 5.25 V, 3.3 V and 1.25 V, respectively. VTHRE indicates threshold voltage for the analog signal.

used for frame ground (FGND) and FGND has electrical conduction with chassis of MuTRG-ADTX. The electrical conduction between AGND/DGND and FGND is optional by jumper pins. Finally we decided common ground for AGND/DGND and FGND to obtain stable ground. In addition, we made common ground for MuTRG-ADTX chassis, shield line of the signal cable from MuTr and MuTr-FEE chassis.

Table 3: Layers of MuTRG-ADTX. Components are mounted on both the first layer and the 8th layer.

<table>
<thead>
<tr>
<th>Layer number</th>
<th>Layer user</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>FGND</td>
</tr>
<tr>
<td>2</td>
<td>AGND and DGND (separate)</td>
</tr>
<tr>
<td>3</td>
<td>Signal</td>
</tr>
<tr>
<td>4</td>
<td>AGND and DGND (conducted)</td>
</tr>
<tr>
<td>5</td>
<td>Signal</td>
</tr>
<tr>
<td>6</td>
<td>AGND and 3.3 V</td>
</tr>
<tr>
<td>7</td>
<td>1.25 V, 2.5 V, 5.25 V and supply voltage</td>
</tr>
<tr>
<td>8</td>
<td>FGND</td>
</tr>
</tbody>
</table>

The size of MuTRG-ADTX board is nearly 6U and 2 boards can be contained in one chassis. Fig. 8 is the picture of MuTRG-ADTX board. Each board is capable of processing up to 64 inputs. To avoid possible cross talk between adjacent channels, signal lines are located in parallel with each other and analog and digital part are located separately at top and bottom region in Fig. 8. The minimal required supply voltage was measured to be about 5.7 V and the operating voltage was tuned to be 6.2 V at the board introducing the safety factor of 0.5 V. The current draw is about 2 A and resulting power consumption is calculated to be 12.4 W per board. The chassis has water cooling structure in both sides which keeps the inside below 60 degrees by continuous flow of cooling water. In addition, heat sink are attached to the significant heat source, i.e. regulators.

2.2. Digital part

The main function of the digital part of MuTRG-ADTX is serialization of the input signal. The 64-bit input signal is digitized, serialized and then transmitted to downstream MuTRG-MRG via an optical cable. The serialization leads to a reduction in number of installed signal cables and the optical interface electrically isolates MuTRG-ADTX from downstream not to introduce any possible noise sources for the analog signal.

Analog signal is converted to digital hit information with a threshold set by DAC (MAX5259, MAXIM), which is controlled by FPGA (Field Programmable Gate Array; XC3S1000, Xilinx). Threshold values of 64 channels can be controlled independently, with the voltage ranges from 0 to 125 mV in ~0.5 mV step. The values are written in RAMs inside the FPGA.
and loaded to the daisy-chained eight DAC chips (one DAC distributes to eight channels). The loaded threshold values can be monitored by hit rates which are recorded and displayed in the online monitor during data taking (see Section 3.2.1).

2.2.1. Data serialization

The digitized 64-bit signal is transmitted to FPGA at a rate of the beam clock of \( \sim 9.4 \text{ MHz} \) (106 nsec). For the operation synchronized with the collision rate, the RHIC beam clock is provided to all MuTRG-ADTX from dedicated beam clock distributors via an optical fiber beside the data transfer line (see Fig. 8).

The 64-bit parallel signal in FPGA is reformatted into six sequential 16-bit data including footers to define the boundary of the data of a given beam crossing. This reformat is necessary to utilize TLK1501 (Texas Instruments) which only has 16 input pins. TLK1501 is a serializer and equipped in order to adjust the signal to the input of optical transceiver (AFBR5710LZ, AVAGO). In the process of the reformating, asynchronous crystal clock of 60 MHz is used since TLK1501 requires clean clock with jitter of 40 psec in peak to peak, whereas the jitter of the RHIC beam clock is about 25 psec in RMS. The asynchronous process is realized at FIFO (fast-in-fast-out) modules inside the FPGA. The frequency of input clock for the FIFO is \( 9.4 \times 6 \text{ MHz} \) which is made by PLL (Phase Locked Loop) inside the FPGA from RHIC beam clock. This rate is determined in order to transfer six sequential packets in just proportion. The reformatted 16-bit data are read out from the FIFO with the crystal clock, and sent to TLK1501. The speed of the serialized optical signal to downstream is 1.2 Gbps with data bandwidth of 960 Mbps. This rate is a consequence of 8b/10b encoding implemented in TLK1501.

As a result of the inconsistent frequencies between the input and output clock of the FIFO, MuTRG-ADTX ends up sending empty packets of 3.4 MHz (= 60 – 6 \times 9.4) to its downstream. These packets are however ignored in MuTRG-MRG.

Fig. 9 illustrates the function of FPGA with block diagram of the digital part of MuTRG-ADTX. CPLD (Complex Programmable Logic Device; XC95144XL, Xilinx) and PROM (Programmable Read Only Memory; XCF04S, Xilinx) are equipped for slow control which is described in Section 2.2.2.

2.2.2. Slow control

As it is essential to control functions of MuTRG-ADTX remotely during the beam time, several slow control capabilities are implemented in MuTRG-ADTX. The slow control signal is transmitted from MuTRG-MRG via optical cables. CPLD serves an important role in slow control and receives 16-bit control signal via TLK1501 (Fig. 9). There are two categories of slow control mode. The first one is targeting the FPGA and the second one is targeting the PROM. The target device is identified in CPLD based on a few digits from MSB (Most Significant Bit) of the received 16-bit.

The first category of the slow control includes two writing modes and contents are the following:

- Data transfer mode
- FPGA reset
- Test pulse transfer mode
- Writing test pulse pattern
- Threshold loading
- Writing threshold values

Data transfer mode activates the FPGA function and hit data sent to MuTRG-ADTX is transmitted to MuTRG-MRG. In this mode, either CFD or LED output can be selected as hit data. FPGA reset mode initializes the modules in the FPGA (register, beam clock counter, PLL, FIFO). Test pulse transfer mode is useful for debugging purpose. It generates pre-programmed signal internally which enables us to test the digital part of MuTRG-ADTX without having the signal input from the analog part. The test pulse patterns are written in RAMs inside the FPGA. There are two modes in slow control for the threshold setting. One is threshold loading and the other is threshold writing to the RAM.

The second category is writing the FPGA design to the PROM. The FPGA design is transmitted in JTAG protocol from MuTRG-MRG via an optical cable and written to the PROM [12]. The design is loaded to the FPGA automatically when MuTRG-ADTX power is turned on.

2.3. Production and installation

The mass production of MuTRG-ADTX boards were carried out in Japan, then they were shipped to BNL. All 400 boards, including 10% spare boards, were tested both at RIKEN, Japan and BNL, US before installation using test pulse. The items examined by the test are listed below.

- Data transfer mode
- FPGA reset
- Test pulse transfer mode
- Writing test pulse pattern
- Threshold loading
- Writing threshold values

As a result of the inconsistent frequencies between the input and output clock of the FIFO, MuTRG-ADTX ends up sending empty packets of 3.4 MHz (= 60 – 6 \times 9.4) to its downstream. These packets are however ignored in MuTRG-MRG.

Fig. 9 illustrates the function of FPGA with block diagram of the digital part of MuTRG-ADTX. CPLD (Complex Programmable Logic Device; XC95144XL, Xilinx) and PROM (Programmable Read Only Memory; XCF04S, Xilinx) are equipped for slow control which is described in Section 2.2.2.

2.2.2. Slow control

As it is essential to control functions of MuTRG-ADTX remotely during the beam time, several slow control capabilities are implemented in MuTRG-ADTX. The slow control signal is transmitted from MuTRG-MRG via optical cables. CPLD serves an important role in slow control and receives 16-bit control signal via TLK1501 (Fig. 9). There are two categories of slow control mode. The first one is targeting the FPGA and the second one is targeting the PROM. The target device is identified in CPLD based on a few digits from MSB (Most Significant Bit) of the received 16-bit.

The first category of the slow control includes two writing modes and contents are the following:

- Data transfer mode
- FPGA reset
- Test pulse transfer mode
- Writing test pulse pattern
- Threshold loading
- Writing threshold values

Data transfer mode activates the FPGA function and hit data sent to MuTRG-ADTX is transmitted to MuTRG-MRG. In this mode, either CFD or LED output can be selected as hit data. FPGA reset mode initializes the modules in the FPGA (register, beam clock counter, PLL, FIFO). Test pulse transfer mode is useful for debugging purpose. It generates pre-programmed signal internally which enables us to test the digital part of MuTRG-ADTX without having the signal input from the analog part. The test pulse patterns are written in RAMs inside the FPGA. There are two modes in slow control for the threshold setting. One is threshold loading and the other is threshold writing to the RAM.

The second category is writing the FPGA design to the PROM. The FPGA design is transmitted in JTAG protocol from MuTRG-MRG via an optical cable and written to the PROM [12]. The design is loaded to the FPGA automatically when MuTRG-ADTX power is turned on.

2.3. Production and installation

The mass production of MuTRG-ADTX boards were carried out in Japan, then they were shipped to BNL. All 400 boards, including 10% spare boards, were tested both at RIKEN, Japan and BNL, US before installation using test pulse. The items examined by the test are listed below.
Figure 9: The block diagram of the digitized data flow. The main function of the digital part of MuTRG-ADTX is serialization of the input signal. The 64-bit input signal is digitized, serialized and then transmitted to MuTRG-MRG via an optical cable. The data stream is processed by FPGA, CPLD, TLK1501, and optical transceiver (optical transceiver is not drawn in this figure). The asynchronous FIFO switches the operating clock of MuTRG-ADTX from RHIC beam clock to the crystal clock and enable us to operate the TLK1501 located at the downstream of the FPGA. CPLD also plays important role in slow control.

- Gain reduction on MuTr-FEE
- Channel-by-channel cross talk
- Fake hit rate
- Efficiency
- Slow control (reset, threshold setting, PROM configuration)

Failure was detected in 13 boards out of 400 boards in total by this test. Most of the failure mode include broken chip and soldering failure. Finally all boards passed the examination after fixing the problem.

The board production were performed in two periods depending on the installation schedule. The installation of MuTRG-ADTX completed during RHIC shutdown period in 2008 for the North MuTr and in 2009 for the South MuTr. The boards were installed in all three non-stereo cathode planes for Station-1, and two downstream and upstream non-stereo cathode planes for Station-2, and all two non-stereo cathode planes for Station-3. Mechanical structure of the non-stereo cathode strips in the same station is identical and hits of strips from multiple planes which cover same acceptance are merged by taking their OR/AND in the actual operation. This feature provides redundancy to optimize the trigger performance. The installation was carefully performed not to damage existing system and to avoid mis-cabling because we had to disconnect cables between MuTr and existing MuTr-FEE to attach MuTRG-ADTX. We also checked noise on MuTr-FEE, which directly affect position resolution of MuTr. After the installation we examined the MuTRG-ADTX performance with calibration pulse by controlling them using MuTRG-MRG and confirmed all boards worked properly.

3. MuTRG-ADTX performance

The performance of MuTRG-ADTX can be separated into two components; (1) Impact on the existing MuTr-FEE and (2) Performance of MuTRG-ADTX itself. We evaluated the performance of MuTRG-ADTX in several test experiments with beam as well as with cosmic ray and test pulse at a test bench. The results in the following sections include those from such various measurements. Here are the list of such measurements.

- Test bench at Kyoto University and RIKEN with test chamber
- An electron beam test at Tohoku University in 2006
- A cosmic ray test at PHENIX in 2007
- A beam test at PHENIX in 2008 (200 GeV $p\-p$ collision)
- A beam test at PHENIX in 2009 (500 GeV $p\-p$ collision)
- A beam test at PHENIX in 2010 (200 GeV/u Au-Au collision)
- A beam test at PHENIX in 2011 (500 GeV $p\-p$ collision)

Since the development of MuTRG-ADTX had been in progress, the MuTRG-ADTX boards used in those measurements were not identical. The development of the board started with analog and digital part separately to avoid possible noise from digital part to analog part and to make easier to figure out the source of the problem. The board of analog and digital part is named as MuTRG-AD and MuTRG-TX, respectively. Based on the first measurement at the PHENIX detector and confirmation that digital part didn’t affect the performance of analog part, a significant upgrade of combining analog and digital part was decided between two measurements in 2007 and 2008. The final design was fixed after the test measurements in 2008.
3.1. Impact on the existing MuTr-FEE

3.1.1. MIP distribution

MuTr readout system records four ADC samples for each signal as shown in Fig. 10. Pulse height and signal timing can be extracted by fitting the four points to quadratic function in the performance study.\(^2\) Fig. 11 shows typical pulse height distribution for the cathode strips measuring maximum charge in clusters (peak strip). The distribution shows Landau distribution and the typical most probable value (MPV) is 150 channel in ADC.

![Figure 10: MuTr-FEE raw signal. The amplitudes indicated by arrows are digitized and recorded. The location of arrow is 1, 6, 7, and 8 in the unit of beam clock.](image)

![Figure 11: Typical ADC distribution of peak strips.](image)

3.1.2. Charge gain reduction

As described in Section 2.1, MuTRG-ADTX consumes about 5% of the signal charge. As a consequence the gain for the particle energy deposit is reduced at the input of MuTr-FEE. It causes that noise fluctuation becomes relatively larger compared to signal. We will discuss degradation of performance due to increased noise level in Section 3.1.3. Another concern is strip-dependent variety of gain reduction. Because position of particle trajectory is determined by profile of strip-by-strip charge deposit, gain non-uniformity could result in degradation of position resolution, although, in principle, such gain non-uniformity is corrected by calibration pulse. Fig. 12 shows typical pulse height reduction by MuTRG-ADTX installation measured using calibration pulse. The gain on MuTr-FEE is reduced to be about 90% in average. The gain reduction using cosmic ray was also measured at the test in 2007 and was 94%. The reason of gain reduction difference between calibration pulse data and cosmic ray data is supposed to be due to frequency dependence of op-amp gain and different frequency component of calibration pulse and cosmic ray. Variety of the gain reduction over strips turns out to be less than 1% in sigma based on Fig. 12. If the variety is considered as background noise, the corresponding noise level which is discussed in Section 3.1.3 is estimated to be much smaller than 1%, expecting that the calibration with MuTRG-ADTX installed correct the gain reduction variety. Based on Fig. 14, this effect is sufficiently small.

![Figure 12: Pulse height reduction on MuTr-FEE by installing MuTRG-ADTX. Each entry corresponds to the measurement for a strip and, therefore, the width indicates strip-to-strip variety. Data from a certain cathode plane in Station-1 as a typical case.](image)

3.1.3. Noise level

Installing MuTRG-ADTX is equivalent to inserting additional capacitance in view from existing MuTr-FEE. It causes increase of noise on MuTr-FEE which results in degradation of position resolution, therefore it is important to keep noise level as low as possible. Fig. 13 shows the pedestal RMS distribution on MuTr-FEE before and after installing the MuTRG-AD board. The distribution is supposed to represent the size of noise. By installing MuTRG-AD, noise increased by about 30%. The noise increase is smaller at longer strips region because longer strips have originally larger capacitance and rela-
tive increase of capacitance due to MuTRG-ADTX installation is small.

Figure 13: Distribution of the pedestal RMS on MuTr-FEE measured at the test experiment in 2007. Each entry of histograms corresponds to the measurement for a strip. The histograms with dashed line and solid line were measured before and after installing MuTRG-AD board, respectively.

Finally position resolution can be evaluated using noise to signal ratio. We name noise level as the ratio of noise divided by signal pulse height. Fig. 14 shows position resolution as a function of noise level measured in the electron beam test experiment in 2006. The impact of noise increase on the position resolution is described only by noise level and is independent from the installation of the MuTRG-AD board. Based on this results, we concluded that the degradation of the position resolution by installing MuTRG-ADTX can be evaluated using a parameter of the noise level. The noise level was about 1.1 % after installing MuTRG-ADTX boards. This noise level corresponds to the position resolution of about 110 µm based on Fig. 14 and we decided the noise level achieved to the sufficient value. Because the noise level is defined as the noise divided by the signal height, we can improve it by increasing signal pulse height. Raising high voltage of MuTr by 25 V on average can compensate for the 30 % increase of the noise level.

3.1.4. Signal timing

Because of small input capacitance of 56 pF in MuTRG-ADTX, higher frequency current component of the signal charge, mostly rising part, is selectively filtered and processed into MuTRG-ADTX. As a consequence, the signal peak timing on MuTr-FEE is delayed due to smeared rising. The timing distributions of the signal peak on MuTr-FEE between with and without the MuTRG-AD board installed are compared in Fig. 15. The timing shifts by about one beam clock.

Because MuTRG-ADTX was installed in only non-stereo cathode plane but the adjustment knob of the trigger timing for MuTr-FEE readout is common over all cathodes in each station, the trigger timing can not be optimized for all cathode planes. For this reason, we need to evaluate strip-by-strip gain variation due to unoptimized signal timing, though such variation can be canceled by calibration using test pulse to a certain degree. Fig. 16 shows ratio of pulse height on MuTr-FEE with artificial timing shift divided by that with optimized timing. Both the average gain shift and the strip-to-strip variation due to the signal timing shift of one beam clock are smaller than 1 % and can be ignored compared with noise on MuTr-FEE.

3.2. Performance of MuTRG-ADTX

In this section, we concentrate on evaluating the performance of MuTRG-ADTX itself. MuTRG-ADTX has capability of selecting CFD or LED. In this section, the measurement was done with CFD unless otherwise noted. We will compare CFD and LED in Section 3.2.4.
3.2.1. Fake hit rate

Fake hits caused by noise are preferred to be as small as possible because they can produce fake trigger due to random coincidence of 3 stations or random coincidence with beam-related background. Fig. 17 shows fake hit rate as a function of threshold for a typical single strip. The fake hit rate becomes exponentially reduced by increasing threshold. The fake hit rates are slightly higher in the region where longer strips are because the noise are coupled to the size of the capacitance. Based on GEANT simulation, it turns out that the trigger rejection power is kept for the random fake hit rate up to 100 kHz.

3.2.2. Efficiency of each cathode plane

Important performance of MuTRG-ADTX is efficiency because its degradation directly causes inefficiency of the trigger. Fig. 18 shows efficiency turn-on curve for single cathode plane as a function of ADC measured by MuTr-FEE readout. Peak strips of clusters are picked up for the calculation. The efficiency turn-on curve is fitted to Gaussian error function to evaluate its property. The efficiencies at plateau achieved to be more than 90% and the turn-on point, which is the point where the efficiency is half of its plateau, is typically 60 channel in ADC when threshold of 30 mV is applied. The major source of the inefficiency at the plateau is timing cut of three beam clocks which is discussed in Section 3.2.3. Comparing to MPV of ~150 channel in ADC distribution, the turn-on point is sufficiently small. Overall efficiency for the ADC distribution of the peak strip is about 90%. As mentioned in Section 2.3, because MuTRG-ADTX was installed in three planes for Station-1, and two planes for Station-2 and 3, the efficiency is expected to be more than 99% when we require OR of planes. When we require hits in two planes out of three planes for Station-1, the efficiency is expected to be more than 97%.

3.2.3. Signal timing

Fig. 19 shows timing distribution of MuTRG measured with cosmic ray as well as beam collisions at RHIC. The results from cosmic ray data and beam data are consistent with each other. MuTRG alone can not determine a beam crossing at which collision occurs because the timing resolution is over the interval of the beam crossings of 106 nsec. MuTRG system works as trigger by making AND with other trigger with good timing resolution. BBC at low luminosity condition or RPC can provide the trigger timing.

Depending on the timing resolution, the time window to accept signals has to be open widely to achieve high efficiency.

---

1In this paper, Gaussian error function is defined as

\[ A \left[ \frac{1}{2} + \int_{\mu}^{\infty} \frac{1}{\sqrt{2\pi}\sigma} \exp \left( -\frac{(t-\mu)^2}{2\sigma^2} \right) \, dt \right]. \]

A, \mu and \sigma are regarded as fitting parameters and named as plateau, turn-on mean (turn-on point) and turn-on sigma, respectively.
3.2.4. Performance difference of CFD and LED

We adopted LED instead of CFD in the measurement at the 2011 RHIC Run because the faster trigger timing is preferable to install MuTRG to the PHENIX trigger system. We evaluate the performance difference between CFD and LED in this section. The demerits of LED are time walk effect and degradation of timing resolution. Fig. 20 shows MuTRG hit timing as a function of ADC. The time walk effect of about one beam clock is observed in the measurement with LED. The RMS of the hit timing is about one beam clock and is better in CFD by ∼0.1 beam clock than LED. When we applied three beam clock acceptance window for the trigger, the degradation of the efficiency in LED is a few % compared to CFD.

4. MuTRG-MRG board and MuTRG-DCMIF board

A snapshot of the strip hits at each beam clock tick is taken and transferred to the data merger board (MuTRG-MRG, Fig. 21). The MuTRG-MRG board receives data from the MuTRG-ADTX boards at a rate of 1.2 Gbps through optical cables. After merging and reformatting data from multiple MuTRG-ADTX boards, the MuTRG-MRG board sends the hit data sorted by strip number, to the LL1 module at a rate of 2.8 Gbps for the Level-1 trigger decision. The MuTRG-MRG also sends the data to the DCM through an interface board (MuTRG-DCMIF, Fig. 24) upon a Level-1 trigger accept signal from the PHENIX granule timing module (GTM) [7]. The MuTRG-DCMIF board combines triggered data from 8 MuTRG-MRG boards, and sends them to the DCM. The data recorded by the DCM is to be used to monitor and diagnose the trigger electronics in online/offline analyses. Hardware specifications of the MuTRG-MRG and the MuTRG-DCMIF boards are given in Table 4. Detail of the MuTRG-MRG and the MuTRG-DCMIF boards are described in following sections.

4.1. MuTRG-MRG board

4.1.1. Design

Main roles of the MuTRG-MRG are (1) to receive the data from the MuTRG-ADTX and extract hit patterns from them, (2) to transmit the extracted hit patterns to the LL1 module to generate Level-1 trigger signals for high-momentum tracks, (3) to transmit the hit patterns to the PHENIX main data stream as well via the MuTRG-DCMIF for offline analysis and (4) to control the MuTRG-ADTX boards remotely. Fig. 21 shows the MuTRG-MRG board. In order to satisfy the capability of multiple functions required as above, a FPGA (XC3S4000, Xilinx) was employed.

As Fig. 21 shows, the MuTRG-MRG has following I/O channels.
Table 4: Specifications of the MuTRG-MRG and the MuTRG-DCMIF

<table>
<thead>
<tr>
<th></th>
<th>MuTRG-MRG</th>
<th>MuTRG-DCMIF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of modules</td>
<td>64 (32 per arm)</td>
<td>8 (4 per arm)</td>
</tr>
<tr>
<td>I/O</td>
<td>10 (1.2 Gpbs optical link to MuTRG-ADTX)</td>
<td>8 (1.2 Gpbs optical link to MuTRG-MRG)</td>
</tr>
<tr>
<td></td>
<td>1 (2.8 Gpbs optical link to LL1 board)</td>
<td>1 (1.6 Gpbs serial link to DCM)</td>
</tr>
<tr>
<td></td>
<td>1 (0.2 Gpbs serial link to MuTRG-DCMIF)</td>
<td>1 (0.2 Gpbs optical link to GTM)</td>
</tr>
<tr>
<td>Size</td>
<td>VME 9U (160 mm depth)</td>
<td>VME 9U (160 mm depth)</td>
</tr>
<tr>
<td>Voltage</td>
<td>+3.3 V</td>
<td>+3.3 V, +5.0 V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>~4.3 A (in normal operation)</td>
<td>~1.2 A (+3.3 V), ~0.5 A (+5.0 V)</td>
</tr>
</tbody>
</table>

Since the MuTRG-MRG has high speed signal lines, the layout of chips and modules and the circuit wiring on the MuTRG-MRG are to be concerned. Significant high speed lines on the MuTRG-MRG are 2.8 Gbps serial signal lines, between TLK3101 (Texas Instruments) and the optical transceiver for the transmission to the LL1 module, and 140 MHz parallel lines, between the FPGA and the TLK3101. Even little impedance mismatching in these lines causes distortions of the signals. Also ringing due to incorrect termination should be minimized since rising times of the signals are very fast. Taking into account these concerns, the FPGA, the TLK3101 and the optical transceiver are arranged as close to each other as possible, and all edges in corners of the rapid signal lines are made smooth for the impedance matching.

4.1.2. Data handling and data format

The MuTRG-MRG produces a 192-bit hit pattern from the MuTRG-ADTX data. The MuTRG-MRG requires 3.3 V power input. The power line generates about 4.3 A of current in normal operation. The dimensions of the MuTRG-MRG is 9U (400 mm) in height, 160 mm in depth and 1.6 mm in thickness.
Figure 22: Block diagram of data flow in the MuTRG-MRG board from transceiver chips (TLK1501), which receive the MuTRG-ADTX data, to completion of hit data extraction. The first asynchronous FIFO synchronize the data with beam collision frequency (9.4 MHz).

clocks. To accommodate the inadequate timing resolution, the MuTRG-MRG board expands the extracted hit signal for several beam clocks. For example, if we set the timing window to three, the MuTRG-MRG generates artificial signal for additional two beam clocks following the original signal. Therefore, the single MuTRG-ADTX signal is changed to a consecutive three-beam-clock signal. The MuTRG-MRG merges the expanded hit signals from the multiple cathode planes by taking OR/AND for strips which cover same acceptance. This merging scheme is optional and can be controlled through VME to optimize the efficiency and the fake hit rate. For Station-1, intermediate setting of AND2 which requires hits in two planes out of three planes can be selected.

The MuTRG-MRG transmits the merged hit pattern to the LL1 module. The basic idea for the transmission is same as for the MuTRG-ADTX mentioned in Section 2.2.1. The MuTRG-MRG converts the hit pattern into an array of 16-bit data packets and adds a header packet including an event counter value which is sent from the MuTRG-ADTX, an ID number of the MuTRG-MRG board and an error bit. The array of the packets are written to asynchronous FIFO at a rate of 9.4x14 MHz and read with 140 MHz crystal clock. The data read out from the FIFO are sent to a transceiver chip, TLK3101 (Texas Instruments), and it encodes the data into a serial signal at an effective serial rate of 2.8 Gbps, providing 2.24 Gbps of data bandwidth. The encoded signal are transmitted to the LL1 module via an optical transceiver. As a consequence of above processes, the MuTRG-MRG requires 230 – 300 nsec data-processing time.

When the MuTRG-MRG receives a PHENIX Level-1 trigger, the MuTRG-MRG transmits hit patterns associated with the trigger to the MuTRG-DCMIF which transmits the data to the DCM. Fig. 23(a) shows scheme of the transmission to the MuTRG-DCMIF. After the MuTRG-MRG transmits a hit pattern to the LL1 module, the MuTRG-MRG has to retain the pattern until Level-1 trigger decision will be performed and the trigger accept signal will arrive at the MuTRG-MRG. Therefore the MuTRG-MRG has a function to memorize the hit pattern for every collision up to 13 µsec utilizing a shift register. At the Level-1 trigger reception, the MuTRG-MRG accesses to a hit pattern on a corresponding depth of the shift register. This depth is called "latency" and should be fixed during data taking.

It is technically difficult to transmit all hit data associated with a trigger to the downstream MuTRG-DCMIF within 106 nsec interval of the beam clock cycle. Therefore, multiple event buffers are employed on the MuTRG-MRG. The number of the buffers is 8 so that up to consecutive 8 Level-1 triggers can be handled with the buffers. Because the current PHENIX DAQ has up to 5 event buffers and it means the maximum number of consecutive triggers coming to the MuTRG-MRG is 5, the 8 event buffers in the MuTRG-MRG are enough size to process the data in the PHENIX data taking system. Inner structure of each event buffer is shown in Fig. 23(b). To evaluate performances of the MuTRG-FEE in offline analysis, hit patterns for several beam clocks around an event associated with the trigger should be transmitted. The size of the tolerance window of the transmitted data can be set to a range from 1 to 7 beam
clocks through VME. As Fig. 23(b) shows, each event buffer in Fig. 23(a) has \( n \) event registers to store the hit patterns of consecutive \( n \) collisions, where \( n = 1 - 7 \) represents the size of the window. Two multiplexers convert these hit patterns into an array of 16-bit data packets at a rate of 9.4 MHz.

At last, the MuTRG-MRG adds 8-bit information data such as data number, data type flag and error flag to these 16-bit data packets to reformat them to 24-bit data packet array. After adding a packet of the trigger counter value as a header, the data packet array is sent to a transmitter chip, DS99R105 (National Semiconductor), at a rate of 9.4 MHz. They are encoded into a serial signal with an effective serial rate of 244 Mbps, providing 226 Mbps of data bandwidth. The signals are sent to the MuTRG-DCMIF through a category-6 Ethernet cable.

4.1.3. Control signals for the MuTRG-MRG and the MuTRG-ADTX

The MuTRG-MRG requires various kinds of control signals from the MuTRG-DCMIF and the VME-bus. The required signals include 9.4MHz beam clock signal, several reset signals, trigger signal and configuration signals for the FPGA and the PROM on the MuTRG-MRG. These control signals are sent from the MuTRG-DCMIF and/or the VME bus.

As the MuTRG-DCMIF controls the MuTRG-MRG, the MuTRG-MRG controls the MuTRG-ADTX. Since it is not easy to access physically to the volume of the MuTr where the MuTRG-ADTX are installed, this remote control system for the MuTRG-ADTX is important for the MuTRG-FEE system as well as the data process. The detailed description for the control of the MuTRG-ADTX is provided in Section 2.2.2.
4.1.4. Error handling

If some errors happen on the MuTRG-MRG, the MuTRG-MRG indicates the errors with 9 LEDs on the front panel. These indicators help to diagnose any problems on the MuTRG-MRG. The MuTRG-MRG also sends the error signals to the LL1 module and the MuTRG-DCMIF. Some important parts of the error information are sent to the DCM through the MuTRG-DCMIF together with hit data.

4.2. The MuTRG-DCMIF board

4.2.1. Design

Figure 24: the MuTRG-DCMIF board

The MuTRG-DCMIF is an essential board to transmit hit patterns to the DCM at trigger reception for data collection. Fig. 24 shows a picture of the MuTRG-DCMIF board. The MuTRG-DCMIF has main roles such as (1) to transmit the hit patterns from the MuTRG-MRG to the DCM to record the hit patterns and (2) to distribute timing control signals to the MuTRG-MRG and the MuTRG-ADTX. As well as the MuTRG-MRG, the MuTRG-DCMIF merges many input data. In this point of view, the basic concept of the MuTRG-DCMIF design is same as the MuTRG-MRG. The same FPGA as the MuTRG-MRG, namely XC3S4000 (Xilinx), is employed on the MuTRG-DCMIF. The MuTRG-DCMIF requires 3.3 V and 5.0 V power input. The 3.3 V and 5.0 V power lines generate about 1.2 A and 0.5 A of current respectively. Dimension of the MuTRG-DCMIF is 9U (400 mm) × 160 mm × 1.6 mm. The MuTRG-DCMIF has following I/O channels.

- 8 modular connectors for the connection with the MuTRG-MRG.
- An optical transmitter channel for the connection with the DCM.
- An optical receiver channel for the connection with the GTM.
- A VME J1 connector for connection with the VME bus.
- An optical transmitter channel for the connection with the DCM.

4.2.2. Data format

As mentioned in the Section 4.1.2, the MuTRG-MRG sends a serial signal including hit pattern information and a trigger counter value with an effective rate of 244 Mbps. The MuTRG-DCMIF receives the serial signals from 8 MuTRG-MRG boards, which correspond to the hit information for two octants of the MuTr, by using 8 receiver chips, DS99R106 (National Semiconductor). They decode the signals into arrays of 24-bit data packets at a rate of 9.4 MHz. These decoded data arrays are sent to the FPGA on the MuTRG-DCMIF and written to FIFO memories on the FPGA. After a readout controller confirms that all FIFO have valid data, readout of the written data starts. In the read process, a multiplexer aligns output data packets in a fixed format explained in the following.

At first, the multiplexer transmits the trigger counter value as the first packet of output data. Following the trigger counter packet, the multiplexer consecutively sends other 4 header packets including additional event and module information.

After these header packets, the multiplexer reads hit data packets from the FIFO with changing their order according to a suitable format. The size of the data for each event becomes 2 octants × (96 strips for Station-1 + 192 strips for Station-2 + 320 strips for Station-3) = 76 packets, where 1 packet = 16-bit.

At last, error packets, which indicate error flags on the MuTRG-MRG and the MuTRG-DCMIF, and a longitudinal parity packet, which indicates longitudinal parity of all the packets in the event data, are added on the hit data packets to complete making an output data array. As a result, the number of packets in the array for single trigger is 5 (header) + 76 × n (data) + 2 (trailer), where n is the size of the beam clock window for which events are transmitted (n = 1 – 7).

Each data packet of the array is written to latter asynchronous FIFO at a rate of 9.4 × 12 MHz. The written packets are read with 80 MHz crystal clock and sent to a transmitter, TLK2501 (Texas Instruments). The TLK2501 encodes the 16-bit data packets into a serial signal with an effective serial rate of 1.6 Gbps, providing 1.28 Gbps of data bandwidth. The serial signal are sent to the DCM via an optical transceiver.

4.2.3. Control signals for the MuTRG-DCMIF

Timing control signals for the MuTRG-FEE system is originally generated by the GTM. These signals are sent with a serialized line and they are decoded with a deserializer chip, HDMP1024 (Hewlett Packard). Main control signals used in the MuTRG-FEE system are the beam-clock signal, trigger accept signal and several mode bit signals. The mode bit signals are translated into reset signals for the MuTRG-DCMIF, the MuTRG-MRG and the MuTRG-ADTX on the FPGA.
5. Muon Trigger Performance

5.1. Trigger logic

Fig. 25 schematically displays the concept of the high-momentum muon trigger. The trigger is generated based on hits from each channel of MuTRG-ADTX. The basic idea to select high-momentum muons is to find a straight trajectory originated in the collision point from the hits from MuTRG-ADTX. There are several parameters to optimize the trigger performance and they are summarized below. The order of the items corresponds to actual order of the operation. Detailed explanation is provided in the following sections.

1. Threshold for the pulse height. To be balanced between the level of noise and signal hit efficiency. See Section 3.2.1 and 3.2.2.
2. CFD or LED. See Section 3.2.4.
4. OR/AND of hits in multiple cathode planes in the same station. See Section 5.1.2.
5. Clustering on/off. See Section 5.1.3.
6. Trigger map (acceptance window and sagitta). See Section 5.1.4.

5.1.1. Timing window (LL1 width)

As described in Section 3.2.3, because the timing resolution spreads over two to three beam clocks, the hit signal from the MuTr is expanded for several beam clocks on the MuTRG-MRG board to accommodate this effect as described in Section 4.1.2. A correct timing on the spread hit signal is selected by making AND with other timing-sensitive detector like BBC or RPC on the LL1 module.

5.1.2. OR/AND of hits in multiple cathode planes

MuTRG-ADTX boards are installed in three planes for Station-1, and two planes for Station-2 and 3. Because structure of each non-stereo planes are identical, which means corresponding strips in different gaps have the same rapidity and radial coverage, Either OR or AND mode of corresponding strip hits in multiple cathode planes can be selected. OR mode helps to enhance the trigger efficiency but is transparent against noise, while AND mode rejects fake hits, at the cost of efficiency. For Station-1, we have intermediate setting of AND2; requiring two hits out of three planes. This function is implemented in FPGA on MuTRG-MRG. See also Section 3.2.2 regarding the efficiency.

5.1.3. Clustering

Charge deposit by particle penetration on MuTr is shared by consecutive multiple strips (typically a few strips). This group of strips is called cluster. Compared to single strip hit, the cluster hits cause expansion of the acceptance window which results in degradation of the rejection power of the trigger. In order to minimize the defect of the cluster, an approximate center-strip finding algorithm in a given cluster, namely “clustering algorithm”, was implemented in the LL1 module. The examples of the actual clustering are shown in Fig. 26. The detailed method of the algorithm is described below.

**Step 1** If successive hits are found, clustering starts.

**Step 2-1** If number of the successive hits is less than or equal to four, only the center hit is kept while other hits are discarded (Fig. 26-(a)). If number of hits in the group is two or four, only one hit with smaller channel (arbitrary) near the center is kept (Fig. 26-(b)).

**Step 2-2** Due to limited capacity of FPGA on the LL1 board, if number of the successive hits is more than four, the hits are divided into groups with less than or equal to four. Then, the same procedure of Step 2-1 is performed to each of divided sub-groups. (Fig. 26-(c))

This clustering process is carried out for each beam clock tick, after opening timing window as mentioned in Section 5.1.1. It’s to be noted that this clustering algorithm also behaves like the hit multiplicity cut, although it is not implemented in this trigger system because of the limited FPGA capacity. Events with many particles which are not supposed to be W-production events, as well as fake triggers due to possible common noise, are suppressed by the hit multiplicity cut. Note the clustering is also costs the efficiency as described in Section 5.3 (See Table 5).
5.1.4. Trigger map

Finally, after clustering algorithm finished, the trigger decision is made by comparing real hit pattern and the trigger map in the LL1 module. The trigger map consists of the list of possible strip combinations of three stations which line up in a straight line as an indication of a high-momentum track. In reality, taking into account the variation of the collision point as well as multiple scattering in the material between the collision point and MuTr, the map includes combinations which satisfy a finite acceptance window as illustrated in Fig. 25. The additional acceptance window may be introduced to the map to allow not only a straight line but also small curvature of the trajectory. The latter window controls the momentum threshold of the trigger and is determined by deviation from the intersection at Station-2 of the linear interpolation between Station-1 and 3.

The deviation is represented in the unit of number of strips and called $\Delta$strip (See Fig. 3). For example, $|\Delta$strip| ≤ 1 means that we allow three strips around the straight trajectory. Finally, the combinations of hits which are allowable for triggering are extracted based on GEANT simulation and the map is prorgramed in the LL1 module to function as a look-up table.

5.2. MuTRG operation in the 2011 RHIC Run

MuTRG-FEE was installed in the RHIC shutdown period of 2008 and 2009. The first physics data were taken from the operation in the 2011 RHIC Run of polarized proton-proton run. The operating condition is listed below.

- LED as the discriminator method. We adopt faster trigger timing to adjust to the PHENIX trigger system.
- AND2 for Station-1. OR for Station-2 and 3.
- Timing window of three beam clocks.
- Do clustering.
- $|\Delta$strip| ≤ 1 in the trigger map.

In addition to MuTRG-FEE, we utilized MuID and BBC trigger[11] instead of RPC for the physics trigger in the 2011 RHIC Run. The observed performance of the MuTRG-FEE is discussed in the following sections.

5.3. Efficiency for track

As explained in Section 5.1.4, the trigger decision is made by comparing hits of MuTRG-FEE and the trigger map online. To evaluate the MuTRG-FEE efficiency for a given track extracted by MuTr-FEE, the emulation of the trigger decision is performed in the offline analysis using MuTRG-FEE hits recorded into the PHENIX data stream. Any fraction of tracks reconstructed by MuTr-FEE, but not associated with MuTRG-FEE trigger fire can be considered as inefficiency of MuTRG-FEE. Association between hit location of MuTr-FEE and MuTRG-FEE is also required in this procedure to exclude accidental coincidence. Data set accumulated by the conventional MuID&BBC trigger was used for the efficiency evaluation.

Fig. 27 shows the efficiency for tracks as a function of the track momentum measured by the South muon arm in the 2011 RHIC Run. The momentum thresholds for the track, which is represented by turn-on point of the efficiency, are 7.7 GeV\(\text{/c}\) and 4. The efficiencies shown here do not include inefficiency from MuID and BBC.

![Figure 27: The track efficiency measured at proton-proton collisions in the 2011 RHIC Run. Black points are obtained by making association of tracks measured by MuTr and MuTRG-FEE hits in the offline analysis (See text). Red points require the online LL1 fire in addition to the offline association of MuTr tracks and MuTRG-FEE hits.](image)
12.6 GeV/c in momentum for the South and North muon arm, respectively. As designed to be, MuTRG-FEE shows insensitivity to the low momentum tracks where backgrounds dominate and successfully raised momentum threshold of 2.8 GeV/c provided by MuID. The new thresholds are on the other hand, low enough to be the region where $W$ signal becomes dominant. The lower threshold in the South arm compared to the North arm is due to shorter flight path length for the same magnetic field strength as the North arm.

The measured efficiency at plateau is 92 % for the South muon arm, as shown as filled-circle points in Fig. 27, and 87 % for the North muon arm. The source of the inefficiency is evaluated with data and summarized in Table 5. We must note that significant fraction of the high-momentum track samples reconstructed by MuTr must not be real, but so-called fake tracks, taking into account what one expects from cross sections of true high-momentum muon sources. Such the excess is most likely dominated by mis-reconstructed tracks of muons from hadron decays in the volume of MuTr and accidental coincidence of noise or multiple tracks. Somewhat better efficiency for the real high-momentum muons is expected. Unfortunately we do not have enough sample of true high-momentum muons to evaluate the efficiency performance because of smallness of their cross section. Instead, we confirmed the track efficiency of better than 96 % at high-momentum region in the measurements with cosmic ray.

### Table 5: Sources of the inefficiency

<table>
<thead>
<tr>
<th></th>
<th>South</th>
<th>North</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intrinsic inefficiency</td>
<td>1 %</td>
<td>2 %</td>
</tr>
<tr>
<td>AND2 for Station-1</td>
<td>2 %</td>
<td>2 %</td>
</tr>
<tr>
<td>Timing cut of 3 beam clock window</td>
<td>4 %</td>
<td>5 %</td>
</tr>
<tr>
<td>Clustering</td>
<td>2 %</td>
<td>4 %</td>
</tr>
</tbody>
</table>

To obtain the efficiency results of filled-circle points in Fig. 27, only MuTr and MuTRG-FEE hit information recorded by DCM with MuID&BBC trigger were utilized in the offline analysis (See Fig. 4). In the real data taking, events must be triggered by MuTRG-FEE signal through the LL1 module. The points with open circle in Fig. 27, displays the MuTRG-FEE efficiency including the operating rate of the LL1 module. From this data, the LL1 operating rate was evaluated to be 98 % in the 2011 RHIC Run.

### 5.4. Rejection power

Another important concern, as well as the efficiency, to evaluate the performance of the trigger is the rejection power. The rejection power is defined as the ratio of the BBC trigger rate divided by the rate of the trigger of focus. The rejection power of the new $W$ trigger is described as follows.

$$\text{Rejection Power} \equiv \frac{\text{Rate of MuTRG-FEE&BBC&MuID trigger}}{\text{Rate of BBC trigger}}$$

Fig. 28 shows rejection power of the MuID trigger and the MuTRG-FEE trigger as a function of the BBC trigger rate. The curve guides the required rejection capability of the high-momentum muon trigger in order to fit trigger rate to be in the assigned bandwidth limit of PHENIX DAQ of 2 kHz for muon arms.

As can be seen from the figure, MuTRG-FEE enhanced the rejection power by factor of 10 to 40 compared to the conventional MuID trigger and kept the rejection power sufficiently high for the most of the case except for the very high luminosity period, i.e. BBC rate > 3 MHz. The measured rejection power indicates degradation of the trigger performance depending on the beam luminosity. As possible reasons of the luminosity dependence, we consider

- Degradation of MuID trigger rejection power. MuID suffers from ringing noise which generate fake triggers. Such fake triggers starts to make coincidence with beam collisions at high luminosity condition.
- Signal cross talk of MuTr over anode wires. It create fake hits after 30 $\mu$s at the timing of signal undershoot and generate fake triggers. The effect is severe at high luminosity condition.
- Worse beam condition. The beam background is anticipated to be larger with high luminosity and it would generates fake triggers.

We expect that the trigger performance will be improved by making coincidence with RPC trigger which works in high rate condition.

### 6. Summary

We have implemented new electronics to existing signal readout system of muon tracking chambers. The new electronics digitize and process small fraction of the signal charge...
fast enough before the trigger decision in online, providing high momentum trigger based on coarse online tracking from a hit pattern. The new trigger makes the measurement of high momentum muons decayed from W-boson feasible which are overkilled by dominant low momentum backgrounds without it. The new electronics consist of MuTRG-ADTX, MuTRG-MRG and MuTRG-DCMIF. MuTRG-ADTX takes care of signal split for the trigger and analog signal measurement. The back-end electronics MuTRG-MRG receives digitized signal from multiple MuTRG-ADTX boards and transmit these hit information to LL1 module for the trigger decision as well as sending the copy to DCM module via MuTRG-DCMIF for the offline performance analysis. The observed performance from the 2011 RHIC Run demonstrated 85 to 90% trigger efficiencies for the detected high-momentum tracks which are expected to include significant fake tracks. Observed rejection power of new trigger combined with conventional MuID and BBC trigger was satisfactory for most of the 2011 RHIC Run except for very high luminosity period with BBC rate >3MHz. The rejection power will be improved by taking further combination with RPC trigger.

Acknowledgments

We thank the staff of the Collider-Accelerator and Physics Departments at Brookhaven National Laboratory and the staff of the other PHENIX participating institutions for their vital contributions. We acknowledge support for the MuTRG-FEE development from Japanese Ministry of Education, Culture, Sports, Science and Technology (MEIT), and Japan Society for the Promotion of Science, Japan; National Research Foundation and WCU program of the Ministry Education Science and Technology, Korea. We thank RIKEN, Japan; Brookhaven National Laboratory, National Science Foundation (NSF), and University of Illinois at Urbana-Champaign, U.S.A., for the absorber development We also thank NSF, USA, for the development of the MuTRG-LL1 board and RPCs.

References

[12] Xilinx Application Note 058 (XAPP058), Xilinx In-System Programming Using an Embedded Microcontroller